

**Listing of Claims:**

1. (Canceled)
2. (Currently Amended) A data processing device comprising:  
a first circuit configuration (1), which connects a first communication bus (2) with a second  
communication bus (3) and is the bus master of the first communication bus (2);  
a second circuit configuration (4), which is connected with the first communication bus (2),  
wherein the second circuit configuration is equipped with a first output port (5), which is  
connected with the input port (6) of the first circuit configuration (1); and  
Configuration in accordance with claim 1,  
characterized by the fact that  
a third circuit configuration (7) is arranged, which is equipped with a second output port (8) that is connected with the first output port (5) through a logical OR function (9), wherein the output port (10) of the OR function (9) is connected with the input port (6) of the first circuit configuration (1).
3. (Currently Amended) The data processing device of claim Configuration in accordance  
with one of the claims 1 or 2, characterized by the fact that wherein the first circuit configuration  
(1) and the second circuit configuration (4) are separate integrated circuits, which are connected by  
the first communication bus (2) that is arranged on a system board.

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4. (Currently Amended) The data processing device of claim Configuration in accordance with one of the claims 1 or 2, characterized by the fact in that the first circuit configuration (1) and the second circuit configuration (4) are arranged in a joint integrated circuit.

5. (Canceled)

6. (Currently Amended) A method for operating a data processing device, the method comprising the steps of:

(a) providing a first circuit configuration (1) that connects a first communication bus (2) with a second communication bus (3) and that is the bus master of the first communication bus (2), wherein a second circuit configuration (4) is connected with the first communication bus (2) and the second circuit configuration is equipped with an output port (5) that is connected with the input port (6) of the first circuit configuration (1),

(b) generating a wait signal (11) in the second circuit configuration (4);

(c) transmitting the wait signal (11) from the second circuit configuration (4) to the first circuit configuration (1);

(d) allowing the first circuit configuration (1) to wait until the second circuit configuration (4) ends the wait signal (11);

Method in accordance with claim 5,

characterized by the fact that the method characterized by:

arranging a third circuit configuration (7) is arranged, which is equipped with a second output port (8) that is connected with the first output port (5) through a logical OR function (9), wherein the wait signal (11) is sent from the output port (10) of the OR function (9) to the input port

(6) of the first circuit configuration (1) as long as one of the circuit configurations (4,7) transmits a wait signal.

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